Client is in the semiconductor industry by developing strategic competencies, innovative technologies and intellectual property; enabling enterprises to be technologically competitive; and cultivating a technology talent pool to inject new knowledge to the industry.

MICROSYSTEMS, MODULES & COMPONENTS LABORATORY

Senior Research Engineer/Research Officer – 3D TSV consortium

This position deals with the evaluation and characterization of materials required for TSV fabrication and chip to wafer assembly.

Responsibilities:

The key responsibilities will include the selection of materials required for 3D TSV packaging, such as low temperature dielectric deposition PECVD, slurry for Cu CMP, thin wafer handling adhesives, chip to wafer bonding adhesives and wafer level molding. The candidate needs to work with material suppliers and the process team to apply the material successfully for the TSV integration.

Requirements:

- PhD/Master degree in Material Sciences with at least 2 to 3 years relevant experience
- Experience in advanced packaging material evaluation such as dielectric materials, temporary/permanent adhesive, underfill and mold compound
- Hands-on experience on material selection and characterization
- Knowledge of Through Silicon Via process such silicon etching, dielectric deposition, dielectric etching, support wafer system and chip to wafer bonding
- Excellent communication skills and teamwork with strong self-motivation

Interested candidates are invited to submit your latest updated resume stating your availability of employment, current, achievements and expected salary to Adrian Collin Png at: adrian@collincrawford.com